The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HONGJIANG SONG

Appeal No. 2005-1754
Application 09/473,740

ON BRIEF

Before THOMAS, BARRETT, and MACDONALD, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of claims 1 through 20.

Representative claim 1 is reproduced below:

1. A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field.

The following references are relied on by the examiner:

Banker et al. (Banker)	5,497,187	Mar. 5, 1996
Andersson et al. (Andersson)	5,671,249	Sep. 23, 1997
Julyan	5,790,610	Aug. 4, 1998
Lang	5,956,377	Sep. 21, 1999

Claims 1 through 20 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon appellant's admitted prior art in Figure 1 and its corresponding discussion in the Specification as filed in view of Lang as to claims 1 through 8 and 15 through 20. The examiner separately rejects claims 9 through 14 under 35 U.S.C. § 103 as being obvious over appellant's admitted prior art in Figure 1 in view of Lang, further in view of Banker or Andersson or Julyan.

Rather than repeat the positions of the appellant and the examiner, reference is made to the Brief and Reply Brief for appellant's positions, and to the Final Rejection and Answer for the examiner's positions.

OPINION

For the reasons set forth by the examiner in the Final Rejection and Answer, we sustain the two stated rejections of the claims on appeal. We enhance and emphasize the examiner's reasoning with additional reasoning of our own as follows.

At the outset, it is noted that appellant presents arguments only as to independent claims 1, 8 and 15 on appeal in the principal Brief on Appeal. No arguments are presented as to any dependent claim on appeal and no arguments are presented as to the second stated rejection of claims 9 through 14. Therefore, all of the dependent claims on appeal fall with our consideration of their respective independent claims 1, 8 and 15 on appeal.

The claimed buffering approach in each independent claim accommodates different data rates between the first and second buses. Independent claim 1 on appeal further recites "during the buffering, detecting whether at least some of the bits indicate a synchronization field." Correspondingly, a separately recited synchronization detection circuit in claim 8

operates to detect whether some of the received bits indicate a synchronization field "while the data recovery circuit buffering the bits." Lastly, independent claim 15 recites a repeater that "concurrently" buffers the received bits as recited earlier in the claim and it also detects whether at least some of the bits indicated a synchronization field. Thus, each of the independent claims on appeal recite essentially concurrent or overlapping operations occurring substantially at the same time.

It appears to us that the subject matter of independent claims 1, 8 and 15 on appeal do not read over the operation of appellant's admitted prior art Figure 1 to the extent the examiner relies upon this circuit in the formulation of the first stated rejection of some of the claims on appeal. Appellant alleges at page 11 of the Brief that the Background of the Invention "teaches away from detecting whether bits indicate a synchronization field *during* the buffering of the bits to accommodate incoming and outgoing data rates, as the Background section performing the synchronization field detection *after* this buffering." To the extent this characterizes the basic operation of appellant's admitted prior art in Figure 1, this does not

accurately reflect the nature of the subject matter actually recited in the independent claims on appeal.

While the quoted operation may be true for a given set of bits, the claim encompasses appellant's admitted prior art Figure 1 synchronization detection bits operating serially at the same time as other bits are buffered from the incoming data. The buffering operation in prior art Figure 1 in the data recovery circuit DRC occurs during, or while or concurrently with the operation of the synchronization detection circuit 18, even though they may operate in serial manner on different data. The claimed recitations do not distinguish between serial operations upon successive frames of information, as apparently the manner in which Figure 1 operates, versus the situation of which the claimed buffering and detecting of synchronization fields occur in an overlapping manner for a given frame of information. Thus, the independent claims 1, 8 and 15 on appeal do not appear to operate in any manner differently than the admitted prior art. As such, the subject matter of the admitted prior art cannot be fairly stated to teach away from the concurrent operations as alleged from the quoted material at page 11 of the principal Brief on appeal. Based on these views, we do not necessarily

agree with the examiner's characterization that the admitted prior art operates in a manner differently than we have just stated.

On the other hand, to the extent the operation of the claimed invention in independent claims 1, 8 and 15 on appeal may be fairly stated to operate in accordance with the examiner's positions in the Final Rejection and Answer, we agree with the reasoning set forth at pages 2 and 3 of the Final Rejection regarding the combinability of appellant's admitted prior art and the teachings of Lang. In this respect, the paragraph bridging Specification pages 1 and 2 indicates that because the data recovery circuit DRC 16 operates serially with the synchronization detection circuit 18 as noted earlier in this opinion, it is characterized in the first full paragraph at the top of Specification page 2 that significant time delays or latencies are introduced into the operation of the whole circuit in Figure 1. This same operation is aptly characterized at Specification page 3, lines 18-20, with respect to the discussion there of conventional repeater circuits as in Figure 1.

Faced with this observation and notation of what the prior art is well aware of, the examiner's observation is well

taken that it would have been obvious to have employed the teaching of Lang to improve, or otherwise minimize, the delay time of the repeating operation since both the buffering of the bits and the detection of the sync circuit would be performed concurrently according to Lang's teachings. In fact, the last sentence of the Abstract of Lang makes mention of "a method for synchronizing frames in a continuous stream of digital data while minimizing delay in processing the audio data in a radio communication system" (emphasis added). A corresponding statement is made in the paragraph bridging columns 2 and 3 of Lang. With respect to the operation of Figure 3, and in association with the showing of TABLE 2 bridging columns 5 and 6 of Lang, it is stated at column 5, lines 39-41, that "[s]canning is continually performed by FIFO buffer **201**, SYNC template register **202** and comparator **203**, in combination." Even an inspection of the architecture of Figure 3 of Lang indicates that the FIFO buffer 201 operates concurrently with the comparator operation in comparator 203 with respect to SYNC template 202. Thus, the examiner's observation of concurrent operation is plainly shown to the artisan in Figure 3 and discussed in these quoted portions of the reference.

All of this is significant in the context of Lang because of the discussion beginning at line 50 of column 1 of Lang that the prior art approach has built in significant inherent delays for which the invention in Lang is to overcome and minimize. This minimization is discussed as relied upon by the examiner beginning at column 2, line 10. Since Lang operates in a related field of the invention as argued by the examiner in such a manner as to minimize known time delays or latency problems in prior art buffering operations, the teachings of Lang obviously would have been usable by the artisan to have minimized the known latency and time delay problems with respect to appellant's admitted prior art Figure 1. Thus, from Lang, it is apparent to the artisan that buffering the data bits received, and at the same time detecting synchronization fields for those received bits being performed concurrently or in parallel, significantly minimizes any latency or time delay problems of the prior art.

In addition to our disagreement with appellant's views that the admitted prior art teaches away from the claimed invention as expressed earlier in the opinion, we do not agree with the other positions presented by appellant in the principal

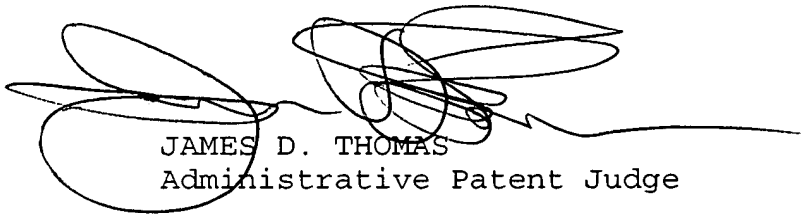
Brief on Appeal. Because the examiner recognizes that Lang's system does not relate to buffering differences and data rates in incoming and outgoing data, the examiner essentially recognizes that Lang's system fails to teach this, contrary to the allegation at the top of page 9 of the principal Brief on Appeal otherwise. The data buffering between incoming and outgoing data rates is argued by the examiner to be taught in the admitted prior art, which is not contested. Nor do we agree with appellant's view that the examiner has exercised prohibited hindsight in formulating the rejections. According to the examiner's view and in contrast to the allegation made at the bottom of page 9 of the principal Brief on Appeal, we have before us a rejection under 35 U.S.C. § 103 relying upon two references and that no single reference has been relied upon by the examiner under 35 U.S.C. § 102 to reject the pending claims on appeal. Since the remarks in the remaining pages of the principal Brief on Appeal parallel those already discussed with respect to independent claim 1, as applied to independent claims 8 and 15 on appeal, the positions in the Brief as to these claims are unpersuasive of patentability.

As to the Reply Brief, we have expanded upon the examiner's reasoning of combinability and the motivations to combine to the extent argued at page 2 of the Reply Brief. Again, our analysis does not conclude that the examiner has exercised prohibited hindsight in formulating the rejecitons. Contrary to the allegation made for the first time at page 2 of the Reply Brief, the combination does produce the claimed invention argued in independent claims 1, 8 and 15 on appeal. Likewise, the examiner's apparent failure as noted at the top of page 3 of the Reply Brief to address appellant's arguments in the principal Brief on Appeal that the admitted prior art teaches away from the claimed invention is not considered fatal as we have discussed earlier in this opinion.

In view of the foregoing, the decision of the examiner rejecting claims 1 through 20 on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED



JAMES D. THOMAS)
Administrative Patent Judge)
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) BOARD OF PATENT
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LEE E. BARRETT) APPEALS AND
Administrative Patent Judge)
) INTERFERENCES
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ALLEN R. MACDONALD)
Administrative Patent Judge)

JDT:psb

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Timothy N. Trop
Trop Pruner Hu & Miles PC
8554 Katy Freeway
Suite 100
Houston, TX 77024